IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

David Goren, et al.

Serial No.: 10/723,752

Filed: November 26, 2003

For: Interconnect-Aware Integrated Circuit Design

Docket No.: IL920030043US1

Examiner:

Group Art Unit: 2825

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF MAILING UNDER 37 CFR 1.8(a)

I hereby certify that the attached correspondence comprising:

1.   Information Disclosure Statement Transmittal Letter;
2.   PTO Form 1449 with 1 reference attached
3.   Return Postcard

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on February 16, 2005.

Jeanne M. Jordan
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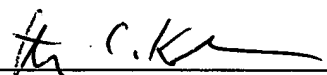Commissioner for Patents
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Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT
TRANSMITTAL LETTER

Sir:

Please find enclosed a listing (PTO Form 1449) of references which may be relevant to the above-referenced application. This listing of references is not a representation that a search has been made, that better references than listed do not exist, or that other references are not applicable. Moreover, this listing does not constitute any admission by applicants or applicants' attorney that the information provided herein is necessarily prior art to applicants' invention. **Please charge any fee necessary to enter this paper to deposit account 09-0468.**

Dated: <u>February 16, 2005</u>   Respectfully submitted,

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FORM PTO-1449 (Modified)	ATTY. DOCKET NO.	SERIAL NO.:
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	IL920030043US1	10/723,752
	APPLICANT: David Goren, et al.	
	FILING DATE: November 26, 2003	GROUP: 2825

REFERENCE DESIGNATION U.S. PATENT DOCUMENTS

EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
	AA	2003/0172358	09/11/2003	Alon et al.			03/06/2002
	AB						
	AC						
	AD						
	AE						
	AF						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	AG							

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

	AI	Goren, D., et al., "On-chip Interconnect-Aware Design and Modeling Methodology, Based on High Bandwidth Transmission Line Devices", DAC 2003, June 2-6, 2003, Anaheim, CA, USA, Copyright 2003 ACM 1-58113-688-9/03/0006
	AJ	
	AL	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.